**Control Signal for Pipeline Processor**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | **EX** | | | | **MEM** | | | **WB** | |
| **Reg Dst** | **ALU Op1** | **ALU Op0** | **ALU Src** | **Branch** | **Mem Read** | **Mem Write** | **Reg Write** | **Mem to Reg** |
| **R-format** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **lw** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **1** | **1** |
| **sw** | **x** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **x** |
| **beq** | **x** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **x** |
| **I-format** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **1** | **0** |